Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	400	717/151.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/02 11:48
L2	141	717/151.ccls. and ("instruction set" or isa)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/02 11:56
L3	121	717/151.ccls. and ("instruction set" or isa) and (compress$3 or reduc$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/02 11:49
L4	0	717/151.ccls. and ("instruction set" or isa) and "static frequency"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/02 11:49
L5	9	("instruction set" or isa) and "static frequency"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/02 11:49
L6	287	712/210.ccls. and ("instruction set" or isa)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/02 11:57
L7	95	712/210.ccls. and ("instruction set" or isa) and frequency	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/02 11:57
L8	86	712/210.ccls. and ("instruction set" or isa) and frequency and (compress$3 or reduc$3)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/02 11:57
L9	84	712/210.ccls. and ("instruction set" or isa) and frequency and (compress$3 or reduc$3) and ("16" or "14" or "32")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/02/02 11:58

S1	203	717/151.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/02/10 12:41
S2	30112	asic	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/02/10 12:41
S3	4	asic and (second adj (processor adj core)) and die	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/02/10 12:57
S4	161	(synthesizing or systhesis) near3 (integrated adj circuit)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/02/10 12:58
S5	19	(synthesizing or systhesis) near3 (integrated adj circuit) and (functional near3 description)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/02/10 12:58
S6	4	("6678645" "6477683").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/15 15:24
S7	8	("5801958" | "5903475" | "6009256" | "6094726" | "6269467" | "6304837" | "6360353" | "6532561").PN.	USPAT	OR	OFF	2004/04/15 15:21
S8	301	soc and (exten$5 and (instruction adj set))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/15 15:24
S9	1	soc same (exten$5 and (instruction adj set)) same dsp	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/15 15:25
S10	24	soc same (exten$5 and (instruction adj set)) and dsp	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/15 15:25

S11	28	soc same (instruction adj set) same dsp	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/15 15:28
S12	901	(instruction adj set) same dsp	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/15 15:31
S13	2	(generat$3 near3 (instruction adj set)) same dsp	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/15 15:29
S14	359	(instruction adj set) near5 dsp	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/15 15:31
S15	10	((custom$7 or exten$5 or generat$3 or creat$3 or develop$3) near3 (instruction adj set)) near5 dsp	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/15 15:34
S16	3	(compress$3 and ratio) near5 (instruction adj set)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/15 15:38
S17	288	712/226.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/15 15:54
S18	1262	soc and dsp	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/15 15:54
S19	31	(soc and dsp) same ((instruction adj set) or isa)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/15 15:59
S20	4	("5666510" | "6230259" | "6349380" | "6574722").PN.	USPAT	OR	OFF	2004/04/15 15:56

S21	26438	hal	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/15 15:59
S22	198	hal and dsp	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/15 15:59
S23	215	ip adj core	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/15 15:59
S24	48	ip adj core and dsp	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/15 16:01
S25	12	ip adj core and dsp and ((instruction adj set) adj simulator)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/15 16:04
S26	154	((instruction adj set) adj simulator)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/15 16:43
S27	37	dsp and (plurality near3 (processor or pu or (processing adj unit))) near3 (chip or silicon)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/15 16:44
S28	0	"6408428.pn",	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/19 08:28
S29	2	"6408428".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/19 08:28
S30	1	"6408428".pn. and extension	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/19 08:32

S31	1	"6408428".pn. and dsp	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/19 08:33
S32	0	"6408428".pn. and (control or status) adj register	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/19 08:33
S33	0	"6408428".pn. and conditional near3 result	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 08:34
S34	0	"6701515".pn. and conditional near3 result	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 08:35
S35	2	"6701515".pn. and extension	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 08:36
S36	1462	compression adj ratio and 7??/???.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 08:37
S37	315	compression adj ratio and soc	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 08:37
S38	28	compression adj ratio same soc	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 08:38
S39	0	compression adj ratio same soc and extension	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 08:38
S40	1	compression adj ratio same soc and dsp	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 08:39

S41	233	compression adj ratio same (instruction or isa)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 08:39
S42	1	compression adj ratio near5 (instruction or isa) and soc	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 08:39
S43	39	compression adj ratio near5 (instruction or isa)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 08:42
S44	3	determin$3 near3 (compression adj ratio) near5 (instruction or isa)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 08:43
S45	901	determin$3 near3 (compression adj ratio)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 08:43
S46	83	determin$3 near3 (compression adj ratio) and 7??/???.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 08:47
S47	18	determin$3 near3 (compression adj ratio) same (isa or instruction)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 08:49
S48	0	determin$3 near3 (compression adj ratio) same risc	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 08:49
S49	1	determin$3 near3 compression same risc	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 08:50
S50	0	determin$3 near3 (compression near3 (ratio or metric or metadata or meta-data)) same risc	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 08:51

S51	18	determin$3 near3 (compression near3 (ratio or metric or metadata or meta-data)) same (instruction or isa or risc or cisc)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 08:54
S52	1	asic near5 dsp and soc and (extension near3 register)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 08:56
S53	1851	asic near5 dspsame (extension near3 register)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 08:56
S54	2	asic near5 dsp same (extension near3 register)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 08:57
S55	0	(plurality or multiple) near3 dsp same (extension near3 register)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 08:57
S56	416	(plurality or multiple) near3 dsp and extension	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 08:58
S57	5	(plurality or multiple) near3 dsp same extension	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 09:05
S58	5	"5418976".URPN.	USPAT	OR	OFF	2004/04/19 09:00
S59	5	(plurality or multiple or multi) near3 dsp same extension	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 09:09
S60	3	(*6240340 "6009370" "5794165"). pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 09:06
S61	4	("6240340" "6009370" "5794165").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 09:07

S62	3	"6240340".URPN.	USPAT	OR	OFF	2004/04/19 09:08
S63	40008	(plurality or multiple or multi) near3 core	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 09:09
S64	181	(plurality or multiple or multi) near3 core and extension and dsp	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 09:10
S65	154	(plurality or multiple or multi) near3 core and extension and dsp and (ic or asic or chip or die or status)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/19 13:47
S66	147	(plurality or multiple or multi) near3 core and extension and dsp and (ic or asic or chip or die or status) and (slots or opcode or op-code or (operation adj code) or bit or instruction)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/20 07:50
S67	1	"6408428".pn. and (assembly or assembler)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/26 08:48
S68	1	"6408428".pn. and pipelin$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/26 15:41
S69	1	"6408428".pn. and (register or conditional or status)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/04/26 15:43
S70	17	("5361373" "5418976" "6223274" "6266807" "6408382" "6408428" "6477683" "6651160" "6701515"). pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/04/26 17:44
S71	2	"6408428".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/01 16:35

S72	1	"6587939".pn. and type	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/02 07:41
S73	1	"6408428".pn. and risc	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/02 07:44
S74	0	"6408428".pn. and asic	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/02 07:45
S75	0	"6587939".pn. and asic	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/12/02 07:45
S76	430	"5493508" "5535331" "5544067" "5555201" "5801958" "5867399" "6173434" "6324678" "6378123" "6421818" ("6477697" "6760888" "6862563").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/20 17:17
S77	26	("5493508" "5535331" "5544067" "5555201" "5801958" "5867399" "6173434" "6324678" "6378123" "6421818" "6477697" "6760888" "6862563").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/21 09:34
S78	88	dsp same risc and "32" and "16" and ((instruction or "op code" or operation) near3 (frequency or count or benchmark or profil$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/21 10:01
S79	88	dsp same risc and "32" and "16" and ((instruction or "op code" or operation) near3 (frequency or count or benchmark or profil$3)) and (customis$5 or customiz$5 or programmab$5 or configur$7 or reprogramab$5 or reconfigur$7)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/21 08:23
S80	102	dsp same risc and "32" and "16" and ((instruction or "op code" or operation) near3 (frequency or count or benchmark or profil$3)) and (customis$5 or customiz$5 or programmab$5 or configur$7 or reprogramab$5 or reconfigur$7) and ("instruction set" or isa)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/21 10:39

S81	9	metacore	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/21 08:29
S82	0	("6862563").URPN.	USPAT	OR	OFF	2005/06/21 08:33
S83	0	("6862563").URPN.	USPAT	OR	OFF	2005/06/21 08:34
S84	46	("20030208723" | "5361373" | "5404319" | "5450586" | "5491640" | "5493508" | "5502661" | "5535331" | "5537580" | "5544067" | "5555201" | "5696956" | "5748875" | "5801958" | "5812416" | "5819050" | "5819064" | "5841663" | "5854929" | "5854930" | "5867399" | "5870588" | "5898595" | "5994892" | "5999734" | "6006022" | "6026219" | "6035123" | "6110223" | "6173434" | "6182206" | "6195593" | "6226776" | "6269467" | "6317860" | "6321369" | "6324678" | "6360350" | "6378123" | "6385757" | "6408428" | "6421818" | "6457173" | "6477683" | "6477697" | "6637018").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/21 08:35
S85	10	("6408428").URPN.	USPAT	OR	OFF	2005/06/21 08:40
S86	0	("6892293").URPN.	USPAT	OR	OFF	2005/06/21 08:48
S87	0	("6862563").URPN.	USPAT	OR	OFF	2005/06/21 08:50
S88	5	("5537341" | "5550839" | "5673198" | "5815405" | "6408428").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/21 08:54
S89	0	("5493508" "5535331" "5544067" "5555201" "5801958" "5867399" "6173434" "6324678" "6378123" "6421818" "6477697" "6760888" "6862563").pn. and ((dsp same risc) and (("32" and "16") near5 (word or bit or width or length or data or format)) and ((instruction or "op code" or operation) near3 (frequency or count or benchmark or profil$3)) and (customis$5 or customiz$5 or programmab$5 or configur$7 or reprogramab$5 or reconfigur$7))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/21 09:39

S90	2	"5794003".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/21 09:38
S91	2	"6892293".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/21 09:38
S92	17	("5493508" "5535331" "5544067" "5555201" "5801958" "5867399" "6173434" "6324678" "6378123" "6421818" "6477697" "6760888" "6862563").pn. and ((dsp or risc) or (("32" and "16") near5 (word or bit or width or length or data or format)) or ((instruction or "op code" or operation) near3 (frequency or count or benchmark or profil$3)) or (customis$5 or customiz$5 or programmab$5 or configur$7 or reprogramab$5 or reconfigur$7))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/21 09:50
S93	2	"5760888".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/21 09:51
S94	0	"mixed a6 bit and 32 bit " and "instruction set"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/21 09:51
S95	0	"mixed 16 bit and 32 bit " and "instruction set"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/21 09:51
S96	0	"16 bit and 32 bit " and "instruction set"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/21 09:52
S97	17138	("16" and "32") near3 (bit or width or length or format or data) and (instruction or isa)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/21 09:54

S98	7382	("16" and "32") near3 (bit or width or length or format or data) and ("instruction set" or isa)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/21 09:55
S99	1944	(("16") near3 (bit or width or length or format or data)) and (("32") near3 (bit or width or length or format or data)) same ("instruction set" or isa)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/21 09:57
S100	1629	(("16") near3 (bit)) and (("32") near3 (bit)) same ("instruction set" or isa)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/21 09:58
S101	1567	(("16") near2 (bit)) and (("32") near2 (bit)) same ("instruction set" or isa)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/21 09:58
S102	690	("16-bit" and "32-bit") same ("instruction set" or isa)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/21 09:59
S103	588	("16-bit" and "32-bit") same ("instruction set" or isa) and (customis$5 or customiz$5 or programmab$5 or configur$7 or reprogramab$5 or reconfigur$7)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/21 10:00
S104	118	("16-bit" and "32-bit") same ("instruction set" or isa) and (customis$5 or customiz$5 or programmab$5 or configur$7 or reprogramab$5 or reconfigur$7 or optimiz$5) near3 ("instruction set" or isa)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/21 10:00
S105	8	(frequency or count or benchmark or profil$3) near3 instruction and S104	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/21 10:36
S106	45	tricore	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/21 10:38
S107	2969	"variable length encoding"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/21 10:39

S108	5	dsp same risc and "variable length encoding" and ((instruction or "op code" or operation) near3 (frequency or count or benchmark or profil$3)) and (customis$5 or customiz$5 or programmab$5 or configur$7 or reprogramab$5 or reconfigur$7) and ("instruction set" or isa)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/21 10:40
S109	41	("5982459").URPN.	USPAT	OR	OFF	2005/06/21 11:00
S110	1	("6862563").pn.	USPAT	OR	OFF	2005/06/21 13:29
S111	2	xtensa and mac16	USPAT	OR	OFF	2005/06/21 13:30
S112	5	risc and mac16	USPAT	OR	OFF	2005/06/21 13:54
S113	0	risc and tensa	USPAT	OR	OFF	2005/06/21 15:13
S114	279581	packed word	USPAT	OR	OFF	2005/06/21 15:14
S115	169	"packed word" and "instruction set"	USPAT	OR	OFF	2005/06/21 15:14
S116	165	"packed word" and "instruction set" and "16" and "32"	USPAT	OR	OFF	2005/06/21 15:15
S117	135	"packed word" and "instruction set" and "16" and "32" and (customis$5 or customiz$5 or programmab$5 or configur$7 or reprogramab$5 or reconfigur$7)	USPAT	OR	OFF	2005/06/21 15:28
S118	92	"packed word" and "instruction set" and "16" and "32" and (customis$5 or customiz$5 or programmab$5 or configur$7 or reprogramab$5 or reconfigur$7) near3 (cpu or processor or dsp or isa or "instruction set")	USPAT	OR	OFF	2005/06/21 15:49
S119	269	"half word" and "instruction set" and "16" and "32" and (customis$5 or customiz$5 or programmab$5 or configur$7 or reprogramab$5 or reconfigur$7) near3 (cpu or processor or dsp or isa or "instruction set")	USPAT	OR	OFF	2005/06/21 17:23

S120	3	"quarter word" and "instruction set" and "16" and "32" and (customis$5 or customiz$5 or programmab$5 or configur$7 or reprogramab$5 or reconfigur$7) near3 (cpu or processor or dsp or isa or "instruction set")	USPAT	OR	OFF	2005/06/21 15:50
S121	0	"1/4 word" and "instruction set" and "16" and "32" and (customis$5 or customiz$5 or programmab$5 or configur$7 or reprogramab$5 or reconfigur$7) near3 (cpu or processor or dsp or isa or "instruction set")	USPAT	OR	OFF	2005/06/21 15:50
S122	0	"half word" and "instruction set" and "16" and "32" and (customis$5 or customiz$5 or programmab$5 or configur$7 or reprogramab$5 or reconfigur$7) near3 (cpu or processor or dsp or isa or "instruction set") and "16 bit" and "32 bit"	USPAT	OR	OFF	2005/06/21 15:51
S123	0	"half word" and "instruction set" and "16" and "32" and (customis$5 or customiz$5 or programmab$5 or configur$7 or reprogramab$5 or reconfigur$7) near3 (cpu or processor or dsp or isa or "instruction set") and "16 bit"	USPAT	OR	OFF	2005/06/21 15:51
S124	184	"half word" and "instruction set" and "16" and "32" and (customis$5 or customiz$5 or programmab$5 or configur$7 or reprogramab$5 or reconfigur$7) near3 (cpu or processor or dsp or isa or "instruction set") and ("16" near3 word) and ("32" near3 word)	USPAT	OR	OFF	2005/06/21 17:11
S125	0	"6101592".pn. and risc	USPAT	OR	OFF	2005/06/21 17:11
S126	4	manarray and risc	USPAT	OR	OFF	2005/06/21 17:11
S127	153	"half word" and "instruction set" and "16" and "32" and (customis$5 or customiz$5 or programmab$5 or configur$7 or reprogramab$5 or reconfigur$7) near3 (cpu or processor or dsp or isa or "instruction set") and risc	USPAT	OR	OFF	2005/06/21 17:23

S128	299	(risc or "reduced instruction set") and ((plurality or "one or more") near3 slot)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 13:54
S129	11	(risc or "reduced instruction set") same ((plurality or "one or more") near3 slot)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 13:42
S130	70	(risc or "reduced instruction set") and ((plurality or "one or more") near3 slot) and ("16" near2 bit) and ("32" near2 bit)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 13:55
S131	58	(risc or "reduced instruction set") and ((plurality or "one or more") near3 slot) and ("16" near2 bit) and ("32" near2 bit) not vliw	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 14:01
S132	9	(risc or "reduced instruction set" or sparc or motorola or powerpc) and ((plurality or "one or more") near3 slot) and ("16" near2 bit) and ("32" near2 bit) not vliw and ((compress$3 or exten$4) near2 instruction)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 14:11
S133	10	(risc or "reduced instruction set" or sparc or motorola or powerpc) and ((plurality or "one or more" or multiple or sequence or arrangement) near3 slot) and ("16" near2 bit) and ("32" near2 bit) not vliw and ((compress$3 or exten$4) near2 instruction)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 14:53
S134	2	"6408428".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 14:11
S135	29	(risc or "reduced instruction set" or sparc or motorola or powerpc) and ((plurality or "one or more" or multiple or sequence or arrangement) near3 slot) not vliw and ((compress$3 or exten$4) near2 instruction)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 14:23
S136	6	("6853970" "6490716" "6629312").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 14:26

S137	50	(risc or "reduced instruction set" or sparc or motorola or powerpc) and ((plurality or "one or more" or multiple or sequence or arrangement) near3 slot) and (optimiz$5 or optimis$5) near3 (processor or core or asic or asip or "instruction set")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 14:55
S138	42	(risc or "reduced instruction set" or sparc or motorola or powerpc) and ((plurality or "one or more" or multiple or sequence or arrangement) near3 slot) and (optimiz$5 or optimis$5) near3 (processor or core or asic or asip or "instruction set") not vliw	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 15:17
S139	61	(risc or "reduced instruction set" or sparc or motorola or powerpc) and ((plurality or "one or more" or multiple or sequence or arrangement) near3 slot) and (optimiz$5 or optimis$5 or compress$3) near3 (processor or core or dsp or ic or asic or asip or "instruction set") and (extension or extended) not vliw	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 15:35
S140	61	(risc or "reduced instruction set" or sparc or motorola or powerpc) and ((plurality or "one or more" or multiple or sequence or arrangement) near3 slot) and (optimiz$5 or optimis$5 or compress$3) near3 (processor or core or dsp or ic or asic or asip or "instruction set") and (extension or extended) not vliw and (encod$3 or opcode or slot)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 15:22
S141	3541	(risc or "reduced instruction set" or sparc or motorola or powerpc) and (optimiz$5 or optimis$5 or compress$3 or programmable or configur$5 or reprogrammable or reconfigurable) near3 (processor or core or dsp or ic or asic or asip or "instruction set") and (extension or extended) not vliw and (instruction or isa)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 15:36

S142	203	(risc or "reduced instruction set" or sparc or motorola or powerpc) and (optimiz$5 or optimis$5 or compress$3 or programmable or configur$5 or reprogrammable or reconfigurable) near3 (processor or core or dsp or ic or asic or asip or "instruction set") same (extension or extended) not vliw and (instruction or isa)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 15:40
S143	32	xtensa	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/22 15:40
S144	46	("20030208723" | "5361373" | "5404319" | "5450586" | "5491640" | "5493508" | "5502661" | "5535331" | "5537580" | "5544067" | "5555201" | "5696956" | "5748875" | "5801958" | "5812416" | "5819050" | "5819064" | "5841663" | "5854929" | "5854930" | "5867399" | "5870588" | "5898595" | "5994892" | "5999734" | "6006022" | "6026219" | "6035123" | "6110223" | "6173434" | "6182206" | "6195593" | "6226776" | "6269467" | "6317860" | "6321369" | "6324678" | "6360350" | "6378123" | "6385757" | "6408428" | "6421818" | "6457173" | "6477683" | "6477697" | "6637018").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/22 15:47
S145	12	("4992934" | "5301325" | "5307492" | "5339238" | "5396631" | "5450575" | "5598560").PN. OR ("6035123"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/06/22 16:08
S146	179	(opcode or "operation code") near3 (lsb or (last near2 bits) or "least significant bit")	US-PGPUB; USPAT; USOCR	OR	ON	2005/06/22 16:09
S147	120	(opcode or "operation code") near3 (lsb or (last near2 bits) or "least significant bit") and risc	US-PGPUB; USPAT; USOCR	OR	ON	2005/06/22 18:22
S148	1	"6477683".pn. and dsp	US-PGPUB; USPAT; USOCR	OR	ON	2005/06/22 18:31

S149	1	"6477683".pn. and register	US-PGPUB; USPAT; USOCR	OR	ON	2005/06/23 07:59
S150	0	"6477683".pn. and "status register "	US-PGPUB; USPAT; USOCR	OR	ON	2005/06/23 08:44
S151	1	"5594813".pn.	US-PGPUB; USPAT; USOCR	OR	ON	2005/06/23 08:44
S152	37	("5594813").URPN.	USPAT	OR	OFF	2005/06/23 08:46
S153	0	"6587939".pn. and (asic or ic or circuit)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/27 09:21
S154	1	"6477683".pn. and (asic or ic or circuit)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/27 12:09
S155	16709	encod$3 near2 (register or source or field)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/27 12:10
S156	2720	encod$3 near2 (register or source or field) and (configur$5 or design$3 or program$5) near2 (processor or circuit or dsp or fpga)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/27 12:12
S157	3254	encod$3 near2 (register or source or field) and (configur$5 or design$3 or program$5) near2 (processor or circuit or dsp or fpga) and (msb or lsb or bit or location)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/27 12:13
S158	19	encod$3 near2 (register or source or field) and (configur$5 or design$3 or program$5) near2 (processor or circuit or dsp or fpga) and (msb or lsb or bit or location) and 716/?.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/06/27 12:14
S159	115	712/203.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/24 15:45

S160	103	712/203.ccls. and ("multi-bit" or offset or "multi-use" or "register opcode" or "14" or "15")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/24 15:46
S161	102	712/203.ccls. and ("multi-bit" or "multi-use" or "register opcode" or "14" or "15")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/24 16:09
S162	1076	(defin$3 or specify$3 or specification) near2 "instruction set"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/24 16:09
S163	371	(defin$3 or specify$3 or specification) adj "instruction set"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/24 16:20
S164	0	(asic) adj "instruction set"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/24 16:20
S165	499	execut$3 near2 ("16" and "32")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/24 16:21
S166	0	execut$3 near2 ("16" and "32") same ("without" near3 (conver$4 or translat$3 or transform$5))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/24 16:23
S167	77	execut$3 near5 ("16" and "32") and ("without" near3 (conver$4 or translat$3 or transform$5))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/24 16:24
S168	0	execut$3 near5 ("16" and "32") same ("without" near3 (conver$4 or translat$3 or transform$5))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/24 16:24
S169	11	compression near5 factorization	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/26 14:07

S170	1	compression near5 factorisation	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/26 14:25
S171	13	compression and factorisation and "14 " and "15" and "16" and "32"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/26 14:25
S172	419	compression and factorization and "14 " and "15" and "16" and "32"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/26 14:32
S173	1	compression same ("14 " and "15" and "16" and "32") and factorization same ("14 " and "15" and "16" and "32")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/26 14:33
S174	7485	compression same ("14 " and "15" and "16" and "32") or factorization same ("14 " and "15" and "16" and "32")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/26 14:36
S175	7464	compression same ("14 " and "15" and "16" and "32") or factorization same ("14 " and "15" and "16" and "32") and (("14 " or "15" or "16" or "32") near2 bit)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/26 14:39
S176	7461	compression same ("14 " and "15" and "16" and "32") or factorization same ("14 " and "15" and "16" and "32") and (("14 " and "15" and "16" and "32") adj bit)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/26 14:42
S177	38	((compression same ("14 " and "15" and "16" and "32")) or (factorization same ("14 " and "15" and "16" and "32"))) and (("14 " and "15" and "16" and "32") adj bit)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/26 14:47
S178	0	((compression same ("14 " and "16" and "32")) or (factorization same ("14 " and "16" and "32"))) and (("14 " and "16" and "32") adj bit) and (("14" near5 (in or within)) near3 ("16" or "32"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/26 14:50
S179	6885	(compression or factorization) and (("14" near5 (in or within)) near3 ("16" or "32"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/26 14:53

S180	17	(compression or factorization) and ((("14" near3 bit) near5 (in or within)) near3 (("16" or "32") near3 bit))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/26 14:53
S181	11	("5784585").URPN.	USPAT	OR	OFF	2006/01/26 16:52
S182	0	execut$3 near5 ("16" and "32") same "without translation"	USPAT	OR	OFF	2006/01/26 16:54
S183	5	execut$3 near5 ("16" and "32") same (mode near3 switch$3)	USPAT	OR	OFF	2006/01/26 17:39
S184	1	"6779101".pn.	USPAT	OR	OFF	2006/01/26 17:39

Published since January 1985 and Published before March 2004
Terms used **compression factorization**

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1 Code compression based on operand factorization
Guido Araujo, Paulo Centoducatte, Mario Cartes, Ricardo Pannain
November 1998 **Proceedings of the 31st annual ACM/IEEE international symposium on Microarchitecture**
Publisher: IEEE Computer Society Press
Full text available: pdf(1.27 MB) Additional Information: full citation, references, citings, index terms

2 Java bytecode compression for low-end embedded systems
Lars Ræder Clausen, Ulrik Pagh Schultz, Charles Consel, Gilles Muller
May 2000 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 22 Issue 3
Publisher: ACM Press
Full text available: pdf(241.04 KB) Additional Information: full citation, abstract, references, citings, index terms, review

A program executing on a low-end embedded system, such as a smart-card, faces scarce memory resources and fixed execution time constraints. We demonstrate that factorization of common instruction sequences in Java bytecode allows the memory footprint to be reduced, on average, to 85% of its original size, with a minimal execution time penalty. While preserving Java compatibility, our solution requires only a few modifications which are straightforward to implement in any JVM used in a low-e ...

Keywords: Java bytecode, code compression, embedded systems

3 Compressing MIPS code by multiple operand dependencies
Kelvin Lin, Chung-Ping Chung, Jean Jyh-Jiun Shann
November 2003 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 2 Issue 4
Publisher: ACM Press

Full text available: pdf(576.31 KB) Additional Information: full citation, abstract, references, index terms

Intuitively, destination registers of some instructions have great possibilities to be used as the source registers of the immediately subsequent instructions. Such destination register/source register pairs have been exploited previously to improve code compression ratio [*compression ratio = (Dictionary Size + Encoded Program Size)/Original Program Size*]. This paper further examines the exploitation of both register and immediate operand dependencies to improve the c ...

Keywords: Code compression, benchmarks, data compression, instruction set architecture

4 A generalized envelope method for sparse factorization by rows

Joseph W. H. Liu

March 1991 **ACM Transactions on Mathematical Software (TOMS)**, Volume 17 Issue 1

Publisher: ACM Press

Full text available: pdf(1.09 MB) Additional Information: full citation, abstract, references, citings, index terms, review

A generalized form of the envelope method is proposed for the solution of large sparse symmetric and positive definite matrices by rows. The method is demonstated to have practical advantages over the conventional column-oriented factorization using compressed column storage or the multifrontal method using full frontal submatrices.

Keywords: elimination tree, envelope method, factorization by rows, sparse matrices

5 Compression of time-dependent geometry

Jerome Edward Lengyel

April 1999 **Proceedings of the 1999 symposium on Interactive 3D graphics**

Publisher: ACM Press

Full text available: pdf(1.32 MB) Additional Information: full citation, references, citings, index terms

6 Session 10B: Power saving techniques for embedded processors: Area and power reduction of embedded DSP systems using instruction compression and re-configurable encoding

Subash Chandar G, Mahesh Mehendale, R. Govindarajan

November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Press

Full text available: pdf(93.34 KB) Additional Information: full citation, abstract, references, citings, index terms

In this paper, we propose a reconfiguration mechanism that allows multiple instruction compression to reduce both code size, which in turn reduces the cost, and (instruction fetch) power, which enhances the battery lifetime, two key considerations in embedded DSP systems. We enhance Texas Instruments DSP core TMS320C27x to incorporate this mechanism and evaluate the improvements on code size and instruction fetch energy using real life embedded control application programs. We show that even wit ...

7 Modeling for text compression
Timothy Bell, Ian H. Witten, John G. Cleary
December 1989 **ACM Computing Surveys (CSUR),** Volume 21 Issue 4
Publisher: ACM Press
Full text available: pdf(3.54 MB) Additional Information: full citation, abstract, references, citings, index terms, review

The best schemes for text compression use large models to help them predict which characters will come next. The actual next characters are coded with respect to the prediction, resulting in compression of information. Models are best formed adaptively, based on the text seen so far. This paper surveys successful strategies for adaptive modeling that are suitable for use in practical text compression systems. The strategies fall into three main classes: finite-context modeling, i ...

8 Compressed Code Execution on DSP Architectures
Paulo Centoducatte, Guido Araujo, Ricardo Pannain
November 1999 **Proceedings of the 12th international symposium on System synthesis**
Publisher: IEEE Computer Society
Full text available: pdf(124.69 KB) Publisher Site Additional Information: full citation, abstract, citings

Decreasing the program size has become an important goal in the design of embedded systems target to mass production. This problem has led to a number of efforts aimed at designing processors with shorter instruction formats (e.g. ARM Thumb and MIPS16), or that can execute compressed code (e.g. IBM CodePack PowerPC). Much of this work has been directed towards RISC architectures though.This paper proposes a solution to the problem of executing compressed code on embedded DSPs. The experimental r ...

9 Code compression: Compiler optimization and ordering effects on VLIW code compression
Montserrat Ros, Peter Sutton
October 2003 **Proceedings of the 2003 international conference on Compilers, architecture and synthesis for embedded systems**
Publisher: ACM Press
Full text available: pdf(334.18 KB) Additional Information: full citation, abstract, references, citings, index terms

Code size has always been an important issue for all embedded applications as well as larger systems. Code compression techniques have been devised as a way of battling bloated code; however, the impact of VLIW compiler methods and outputs on these compression schemes has not been thoroughly investigated.This paper describes the application of single- and multiple-instruction dictionary methods for code compression to decrease overall code size for the TI TMS320C6xxx DSP family. The compression ...

Keywords: VLIW, code compression, compiler optimizations

10 Performance of distributed sparse Cholesky factorization with pre-scheduling
S. Venugopal, V. K. Naik, J. Saltz
December 1992 **Proceedings of the 1992 ACM/IEEE conference on Supercomputing**

Publisher: IEEE Computer Society Press
Full text available: pdf(978.77 KB) Additional Information: full citation, references, citings, index terms

11 The relationship between greedy parsing and symbolwise text compression
Timothy C. Bell, Ian H. Witten
July 1994 **Journal of the ACM (JACM)**, Volume 41 Issue 4
Publisher: ACM Press
Full text available: pdf(1.03 MB) Additional Information: full citation, abstract, references, index terms, review

Text compression methods can be divided into two classes: symbolwise and parsing. Symbolwise methods assign codes to individual symbols, while parsing methods assign codes to groups of consecutive symbols (phrases). The set of phrases available to a parsing method is referred to as a dictionary. The vast majority of parsing methods in the literature use greedy parsing (including nearly all variations of the popular Ziv-Lemp ...

Keywords: Ziv-Lempel compression, adaptive modelling, context modeling

12 Evaluation of a high performance code compression method
Charles Lefurgy, Eva Piccininni, Trevor Mudge
November 1999 **Proceedings of the 32nd annual ACM/IEEE international symposium on Microarchitecture**
Publisher: IEEE Computer Society
Full text available: pdf(1.01 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Compressing the instructions of an embedded program is important for cost-sensitive low-power control-oriented embedded computing. A number of compression schemes have been proposed to reduce program size. However, the increased instruction density has an accompanying performance cost because the instructions must be decompressed before execution. In this paper, we investigate the performance penalty of a hardware-managed code compression algorithm recently introduced in IBM's PowerPC 405. ...

13 A compact row storage scheme for Cholesky factors using elimination trees
Joseph W. Liu
June 1986 **ACM Transactions on Mathematical Software (TOMS)**, Volume 12 Issue 2
Publisher: ACM Press
Full text available: pdf(1.47 MB) Additional Information: full citation, abstract, references, citings, index terms, review

For a given sparse symmetric positive definite matrix, a compact row-oriented storage scheme for its Cholesky factor is introduced. The scheme is based on the structure of an elimination tree defined for the given matrix. This new storage scheme has the distinct advantage of having the amount of overhead storage required for indexing always bounded by the number of nonzeros in the original matrix. The structural representation may be viewed as storing the minimal structure of the given matr ...

14 Heap compression for memory-constrained Java environments
G. Chen, M. Kandemir, N. Vijaykrishnan, M. J. Irwin, B. Mathiske, M. Wolczko
October 2003 **ACM SIGPLAN Notices , Proceedings of the 18th annual ACM SIGPLAN conference on Object-oriented programing, systems, languages, and applications OOPSLA '03**, Volume 38 Issue 11
Publisher: ACM Press
Full text available: pdf(2.14 MB) Additional Information: full citation, abstract, references, citings, index terms

Java is becoming the main software platform for consumer and embedded devices such as mobile phones, PDAs, TV set-top boxes, and in-vehicle systems. Since many of these systems are memory constrained, it is extremely important to keep the memory footprint of Java applications under control.The goal of this work is to enable the execution of Java applications using a smaller heap footprint than that possible using current embedded JVMs. We propose a set of memory management strategies to reduce h ...

Keywords: Java virtual machine, garbage collection, heap, memory compression

15 Light field mapping: efficient representation and hardware rendering of surface light fields
Wei-Chao Chen, Jean-Yves Bouguet, Michael H. Chu, Radek Grzeszczuk
July 2002 **ACM Transactions on Graphics (TOG) , Proceedings of the 29th annual conference on Computer graphics and interactive techniques SIGGRAPH '02**, Volume 21 Issue 3
Publisher: ACM Press
Full text available: pdf(7.79 MB) Additional Information: full citation, abstract, references, citings, index terms

A light field parameterized on the surface offers a natural and intuitive description of the view-dependent appearance of scenes with complex reflectance properties. To enable the use of surface light fields in real-time rendering we develop a compact representation suitable for an accelerated graphics pipeline. We propose to approximate the light field data by partitioning it over elementary surface primitives and factorizing each part into a small set of lower-dimensional functions. We show th ...

Keywords: compression algorithms, image-based rendering, rendering hardware, texture mapping

16 Efficient pattern matching with scaling
Amihood Amir, Gad M. Landau, Usi Vishkin
January 1990 **Proceedings of the first annual ACM-SIAM symposium on Discrete algorithms**
Publisher: Society for Industrial and Applied Mathematics
Full text available: pdf(1.51 MB) Additional Information: full citation, references, citings, index terms

17 A DISE implementation of dynamic code decompression
Marc L. Corliss, E. Christopher Lewis, Amir Roth

June 2003 **ACM SIGPLAN Notices , Proceedings of the 2003 ACM SIGPLAN conference on Language, compiler, and tool for embedded systems LCTES '03**, Volume 38 Issue 7
Publisher: ACM Press
Full text available: pdf(291.52 KB) Additional Information: full citation, abstract, references, citings, index terms

Code compression coupled with dynamic decompression is an important technique for both embedded and general-purpose microprocessors. *Post-fetch decompression*, in which decompression is performed after the compressed instructions have been fetched, allows the instruction cache to store compressed code but requires a highly efficient decompression implementation. We propose implementing post-fetch decompression using *dynamic instruction stream editing* (DISE), a programmable decoder-- ...

Keywords: DISE, code compression, code decompression

18 Homomorphic factorization of BRDFs for high-performance rendering
Michael D. McCool, Jason Ang, Anis Ahmad
August 2001 **Proceedings of the 28th annual conference on Computer graphics and interactive techniques**
Publisher: ACM Press
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A bidirectional reflectance distribution function (BRDF) describes how a material reflects light from its surface. To use arbitrary BRDFs in real-time rendering, a compression technique must be used to represent BRDFs using the available texture-mapping and computational capabilities of an accelerated graphics pipeline. We present a numerical technique, homomorphic factorization, that can decompose arbitrary BRDFs into products of two or more factors of lower dimensionality, each factor de ...

***Keywords**: hardware accelerated rendering and shading*

19 A sub-quadratic sequence alignment algorithm for unrestricted cost matrices
Maxime Crochemore, Gad M. Landau, Michal Ziv-Ukelson
January 2002 **Proceedings of the thirteenth annual ACM-SIAM symposium on Discrete algorithms**
Publisher: Society for Industrial and Applied Mathematics
Full text available: pdf(1.04 MB) Additional Information: full citation, abstract, references, citings

The classical algorithm for computing the similarity between two sequences [36, 39] uses a dynamic programming matrix, and compares two strings of size n in $O(n^2)$ time. We address the challenge of computing the similarity of two strings in sub-quadratic time, for metrics which use a scoring matrix of unrestricted weights. Our algorithm applies to both *local* and *global* alignment computations.The speed-up is achieved by dividing the dynamic programming ...

20 Survey of code-size reduction methods
Árpád Beszédes, Rudolf Ferenc, Tibor Gyimóthy, André Dolenc, Konsta Karsisto
September 2003 **ACM Computing Surveys (CSUR)**, Volume 35 Issue 3

Publisher: ACM Press

Full text available: pdf(443.89 KB) Additional Information: full citation, abstract, references, index terms

Program code compression is an emerging research activity that is having an impact in several production areas such as networking and embedded systems. This is because the reduced-sized code can have a positive impact on network traffic and embedded system costs such as memory requirements and power consumption. Although code-size reduction is a relatively new research area, numerous publications already exist on it. The methods published usually have different motivations and a variety of appli ...

Keywords: code compaction, code compression, method assessment, method evaluation

Results 1 - 20 of 200 Result page: **1** 2 3 4 5 6 7 8 9 10 next